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Experimental Demonstration of a Dynamic 10 Gbit/s WDM Header/Label Recognition Structure

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Abstract—In this paper, we experimentally demonstrate a dynamic wavelength-division-multiplexing (WDM) header/label recognition structure that processes on-the-fly WDM patterns. An Opto-VLSI processor is used to dynamically generate digital phase holograms that control the wavelength components of the label/header to create digital wavelength profiles. An autocorrelation function of a high-peak is generated when a label bit pattern matches a digital wavelength profile. The main attractive feature of using an Opto-VLSI processor is that the lookup table of matching digital wavelength profiles does not need modification when the data bit-rate is upgraded. The dynamic pattern recognition structure is experimentally demonstrated at 10 Gbit/s for 4-, 6-, and 8-bit labels.

Index Terms—Packet switching, pattern recognition, optical communications, optical correlators.

I. INTRODUCTION

OPTICAL packet switching networks are a key technology for realizing next-generation, large capacity, high scalability, and fine granularity optical networks. In conventional optical packet switched networks, packets are converted at each node from the optical domain to the electrical domain in order to process the header and make routing decisions [1]. Moreover, as the number of nodes increases, the lookup time becomes a significant source of latency. To avoid optical-to-electrical conversion, and hence, minimise the lookup time, the use of all-optical correlators for optical header recognition has been proposed and demonstrated [1]–[4].

A promising technique for recognizing optical packet headers on the fly involves the use of time-domain optical correlators to correlate an incoming header pattern with predetermined bit patterns of a lookup table [3], [4]. Each correlator is configured to match a specific header pattern that is assigned to a destination port. An autocorrelation function of a very high-peak is generated whenever the optical header bit pattern matches a

pattern of the lookup table, while for other patterns, only low intensity crosscorrelation functions are produced.

A key challenge in the practical implementation of all-optical header recognition based on wavelength-division-multiplexing (WDM) is the need of an efficient optical processor that independently manipulates WDM channels [3]. On the other hand, the performance of optical packet-switched networks relies heavily on the methods used for encoding, transmitting, and extracting the optical header [5]. Headers and payloads can be transmitted on the same wavelength [5], [6], or on different wavelengths [5], [7]. Also, the payload can be delivered at a designated wavelength while the header is transmitted on multiple wavelengths [8]–[15]. An asynchronous optical packet switched network based on combining wavelength and time for header generation has been reported [15], [16], where payloads is carried on a wavelength while the header is coded on multi-wavelength carrier. Employing multiwavelength header patterns enables the node to quickly and efficiently process the header, and easily differentiate it from the payload and extract it from the packet.

Recently, several schemes for multiwavelength header correlator have previously been proposed, which are based on fibre Bragg gratings (FBGs) [8]–[10], semiconductor optical amplifier (SOA) [11], [12], and serial-to-parallel conversion [13], [14].

In this paper, we propose and experimentally demonstrate a dynamic 10 Gbit/s WDM header/label recognition structure, wherein a bank of correlators is implemented using a single Opto-VLSI-processor [17], [18]. The advantage of using an Opto-VLSI processor is its reconfigurability that enables the synthesis of a dynamic lookup table of wavelength profiles that matches different header bit patterns. This capability enables future network expansion/upgrade to be performed without the need for service interruption. Unlike all other reported optical header recognition techniques that are designed for fixed data bit-rates, Opto-VLSI correlators are transparent to data bit-rates. Note that, for a multiwavelength header/label recognition structure, the optical switch architecture is simple, and does not require a nonlinear optical processing or synchronisation in the correlator for wavelength- and/or time-shifting of individual header bits. As a result, the use of multiwavelength header transmission makes the proposed correlator structure very attractive for ultrahigh-speed optical networks.

The paper is organised as follows: Section II describes the Opto-VLSI processor and its capabilities. In Section III, the

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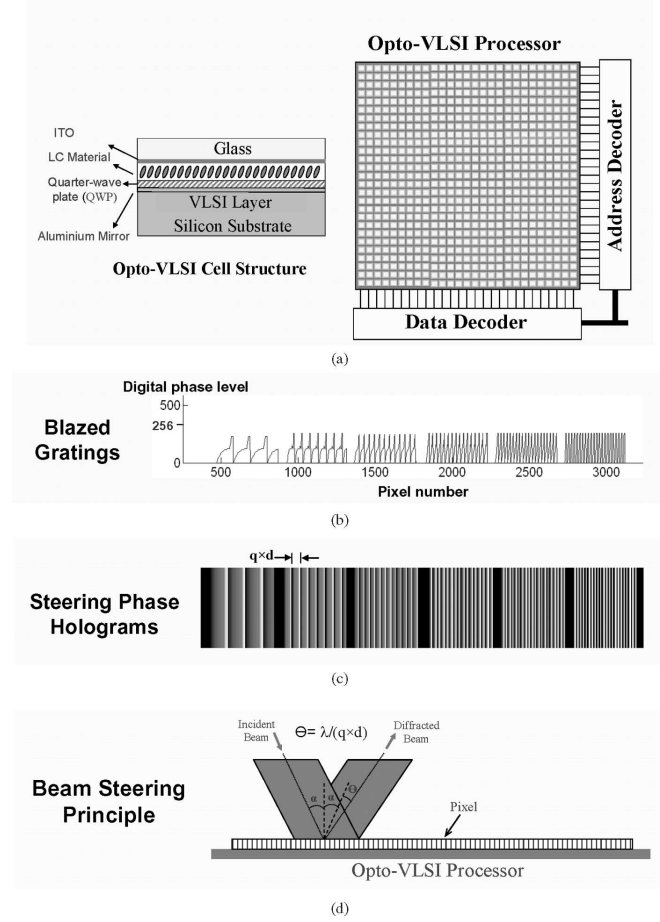


Fig. 1. (a) Opto-VLSI processor structure design. (b) Phase level versus pixel number for blazed grating synthesis. (c) Corresponding steering phase holograms of the various pixel blocks. (d) Principle of beam steering using an Opto-VLSI processor.

multiwavelength dynamic header/label recognition structure is introduced. Section IV presents a theoretical analysis of multiwavelength header recognition structures. The experimental setup and results are presented in Section V, and discussed in Section VI.

II. OPTO-VLSI PROCESSOR

An Opto-VLSI processor comprises an array of liquid-crystal (LC) molecules on a silicon backplane, integrating high-density electronics, and reflective mirrors. The modulation of an incident beam is performed through the change of the orientation of the birefringent ferroelectric or twisted-nematic LC molecules driven by different digital voltages applied to the control electrodes of the Opto-VLSI processor. Due to the different refraction indices of the LC molecules, the incident complex wavefront may undergo a phase shift profile that can steer or reshape the optical beam [17]–[21].

Fig. 1 (a) also shows a typical layout of a 2^N -phase Opto-VLSI processor. Indium-tin oxide (ITO) is used as the transparent electrode, and evaporated aluminum is used as the reflective electrode. By incorporating a thin quarter-wave plate (QWP) layer between the liquid crystal and the VLSI backplane, a

polarization-insensitive Opto-VLSI processor can be realized, allowing optical beam steering with polarization-dependent loss as low as 0.5 dB as reported by Manolis *et al.* [22]. The ITO layer is generally grounded and a voltage is applied at the reflective electrode by the VLSI circuit below the LC layer to generate stepped blazed gratings for optical beam steering [17]–[21].

The steering capability of a typical Opto-VLSI processor of pixel size d , driven by various blazed gratings is shown in Fig. 1(b)–(d). Fig. 1(b) shows different steering phase level profiles and Fig. 1(c) shows the corresponding phase holograms. For a blazed grating pitch of $q \times d$, the optical beam is steered by an angle Θ , i.e., is proportional to the wavelength (λ) of the incident light and inversely proportional to that pitch, as shown in Fig. 1(d). A blazed grating of arbitrary pitch can directly be generated by digitally driving a block of pixels with appropriate phase levels (controlled by changing the voltage applied to each pixel), thus, an incident optical beam is dynamically steered along arbitrary directions.

For a small incidence angle, the maximum steering angle of the Opto-VLSI processor is given by [19]

$$\theta_{\max} \approx \frac{\lambda}{Md} \quad (\text{Radians}) \quad (1)$$

where M is the number of phase levels, d is the pixel size, and λ is the wavelength of the incident beam. For example, a 4-phase Opto-VLSI processor having a pixel size of $5 \mu\text{m}$ can steer a 1550 nm laser beam by a maximum angle of around $\pm 4^\circ$. The maximum diffraction efficiency of an Opto-VLSI processor depends on the number of discrete phase levels that the VLSI can accommodate. The theoretical maximum diffraction efficiency is given by [23]

$$\eta = \text{sinc}^2 \left(\frac{\pi n}{M} \right) \quad (2)$$

where $n = gM + 1$ is the diffraction order ($n = 1$ is the desired order), and g is an integer. Thus, a four-phase-level Opto-VLSI processor allows for efficiency up to 81%. The higher diffraction orders (which correspond to the cases $g \neq 0$) are unwanted crosstalk, which are usually attenuated or properly routed outside the output ports to maintain a high signal-to-crosstalk performance.

III. DYNAMIC WDM HEADER/LABEL RECOGNITION STRUCTURE

In a multiwavelength header/label network, the payload is transmitted on a wavelength λ_0 , whereas the header/label pattern modulates wavelength division multiplexed optical carriers ($\lambda_1, \lambda_2, \dots, \lambda_N$). The structure of the proposed dynamic multiwavelength header/label recognition structure employs an Opto-VLSI processor in conjunction with an array of FBGs of different Bragg wavelengths as shown in Fig. 2. The FBG array is designed to match the header/label wavelengths ($\lambda_1, \lambda_2, \dots, \lambda_N$). The FBGs are equally spaced with a spacing corresponding to half of the bit time of the header (the total delay increment of a round trip is one bit time).

The Opto-VLSI processor is used to generate the routing lookup table through spectral masking of the header

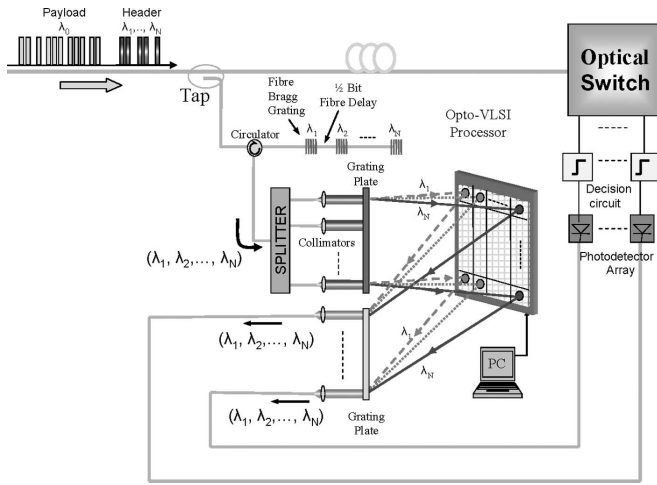


Fig. 2. Dynamic multiwavelength header/label recognition structure.

wavelengths with digital phase holograms (wavelength profile). The active window of the Opto-VLSI processor is logically partitioned into rows of pixel blocks, where each pixel block representing different wavelength, driven by a digital phase hologram. An autocorrelation function is generated when the header wavelengths matches the wavelengths profile.

When a packet with multiwavelength label arrives to the node, a small portion is tapped off and routed to the FBG array using a circulator. The FBG array delays each wavelength by a bit time. Upon reflection off the Bragg gratings, the WDM components of the header are equally split horizontally, collimated, and then, the WDM channels are spatially demultiplexed by a grating plate along different directions and mapped onto N pixel blocks on a 2-dimensional Opto-VLSI processor, where the active window of the Opto-VLSI processor is logically partitioned into rows of pixel blocks. A wavelength component incident on a pixel block can either be steered along a specific optical path, thus, coupled through another grating plate, which multiplexes the WDM channels into the output fibre collimator, or deliberately steered “off-track” so that its power is not coupled back into the fibre collimator. By loading the pixel blocks with optimized digital phase holograms, the intensities of the different wavelengths reflected off the pixel blocks of a row can be arbitrarily attenuated to realise a wavelength profile that matches a specific header/label pattern. Since the wavelengths had been delayed by one bit time increments, an autocorrelation function exhibiting a high-peak at its centre of symmetry is detected by the photodetector when the header bit pattern matches the wavelength profile generated by the Opto-VLSI processor. By comparing the photodetected signal to a threshold level, an electrical signal is generated, which drives the switch to route the individual optical packet. On the other hand, if the header bit pattern does not match the wavelength profile, the correlator output exhibits no spike (crosscorrelation), and hence, the header pattern is not recognised by the threshold detector.

As shown in Fig. 2, the pixel blocks of a particular row are driven by steering holograms that steer the different wavelengths to a central spot on a 2-D grating that couples them into a fibre

collimator, thus, realising a wavelength profile that matches a specific header pattern. By addressing the pixel blocks of the different rows, multiple patterns can be recognised using a single Opto-VLSI processor. Note that, since the Opto-VLSI processor can synthesise arbitrary wavelength profiles, the proposed correlator structure can be reconfigured to recognise arbitrary header patterns.

IV. THEORETICAL ANALYSIS OF MULTIWAVELENGTH HEADER RECOGNITION STRUCTURES

Consider a broadband light source of a wavelength range $\{\lambda_0 - \lambda_M\}$, modulated by an electrical signal $x(t)$, and propagating through an FBG array composed of $(M + 1)$ uniform gratings written on a single-mode fibre at different locations. A FBG of Bragg wavelength λ_k , reflectivity $R_k(\lambda)$, and bandwidth $\Delta\lambda_k$ reflects a waveband centred at λ_k , and induces an incremental time delay T_k with respect to the delay time induces by an adjacent FBG placed at a distance l_k . This incremental time delay is expressed as

$$T_k = \frac{2n_{\text{eff}}l_k}{c} \quad (k = 1, 2, \dots, M) \quad (3)$$

where c is the speed of light in free space, and n_{eff} is the effective refractive index of the fibre.

If $x(t)$ is a data signal, it can be expressed as

$$x(t) = \sum_{k=0}^M m_k r(t - kT) \quad (4)$$

where $r(t)$ is the bit shape (eg., rectangular, Gaussian). The effective power intensity of the modulated light reflected off the k th FBG can be written as

$$P_k = \int_{\lambda_k - 0.5\Delta\lambda_k}^{\lambda_k + 0.5\Delta\lambda_k} P(\lambda) d\lambda R_k \eta x(t) \quad (5)$$

where $P(\lambda)$ is the optical power spectrum density at wavelength λ , and η is the modulator conversion efficiency (defined as the ratio of output ac power to input ac electric voltage).

After reflection by the FBG, the optical power of the modulated light is expressed as

$$P_R = \sum_{k=0}^M \int_{\lambda_0, \Delta\lambda_0} P(\lambda) R_k(\lambda) d\lambda \eta m_k r(t - kT). \quad (6)$$

The Opto-VLSI processor generate a multiwavelength profile, denoted $\{p_0, p_1, \dots, p_M\}$, by significantly attenuating some of the input wavelengths while keeping the other wavelengths intact. The photocurrent produced by the photodetector is given by

$$I(t) = \Re \sum_{n=0}^M p_n \sum_{k=0}^M m_k r(t - nT - kT) \int_{\lambda_0, \Delta\lambda_0} P(\lambda) R_k(\lambda) d\lambda \quad (7)$$

where \Re is the responsivity of the photodetector. If the multiwavelength profile matches the data bit pattern, then $p_k = m_k$ and therefore, (7) becomes the autocorrelation of the data pattern

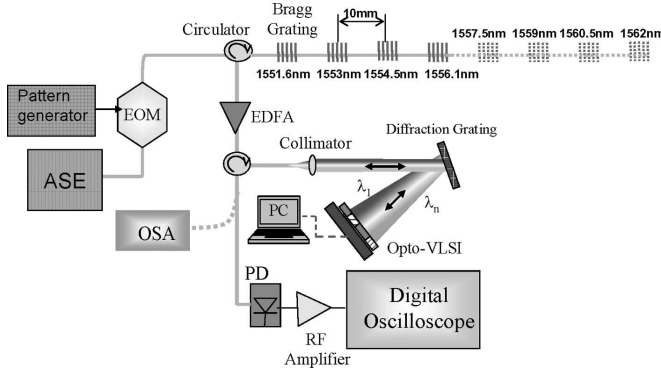


Fig. 3. Experimental setup of the dynamic multiwavelength header/label recognition structure.

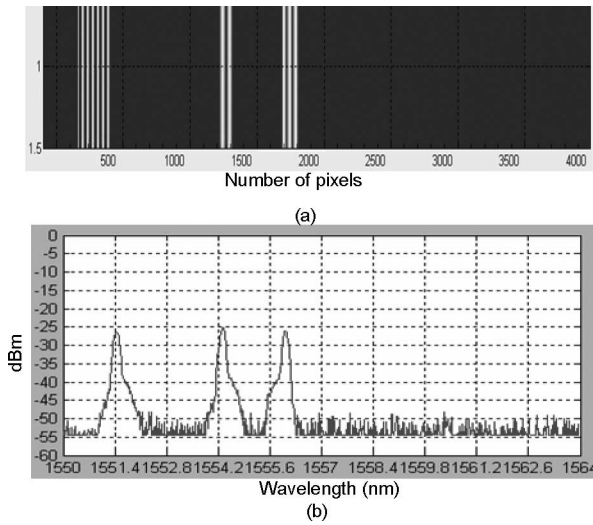


Fig. 4. (a) Opto-VLSI digital hologram of the pixel blocks to generate 1011 wavelength profile. (b) Wavelength profile that matches the optical bit pattern 1011.

$x(t)$. In this case, $I(t)$ becomes the autocorrelation function of $x(t)$, exhibiting a peak at time $t_c = MT$.

V. EXPERIMENT SETUP AND RESULTS

In order to proof the capabilities of the proposed structure, an experiment was setup, as shown in Fig. 3, to demonstrate three scenarios for recognising 4-, 6- and 8-bit patterns.

A -10 dBm low coherence amplified spontaneous emission (ASE) source was launched into an electro-optic modulator (EOM) and intensity-modulated with a 10 Gb/s pattern (4, 6, and 8 bit pattern). The modulated light was launched into an optical fiber having an array of eight FBGs equally spaced, with centre-to-centre at 10 mm. All FBGs had identical reflectivities of 90% and Bragg wavelengths of $\lambda_1 = 1551.6$ nm, $\lambda_2 = 1553$ nm, $\lambda_3 = 1554.5$ nm, $\lambda_4 = 1556.1$ nm, $\lambda_5 = 1557.5$ nm, $\lambda_6 = 1559$ nm, $\lambda_7 = 1560.5$ nm, and $\lambda_8 = 1562$ nm, respectively.

The FBG array spectrally slices an incoming broadband optical signal into eight different wavelengths, with an equal delay

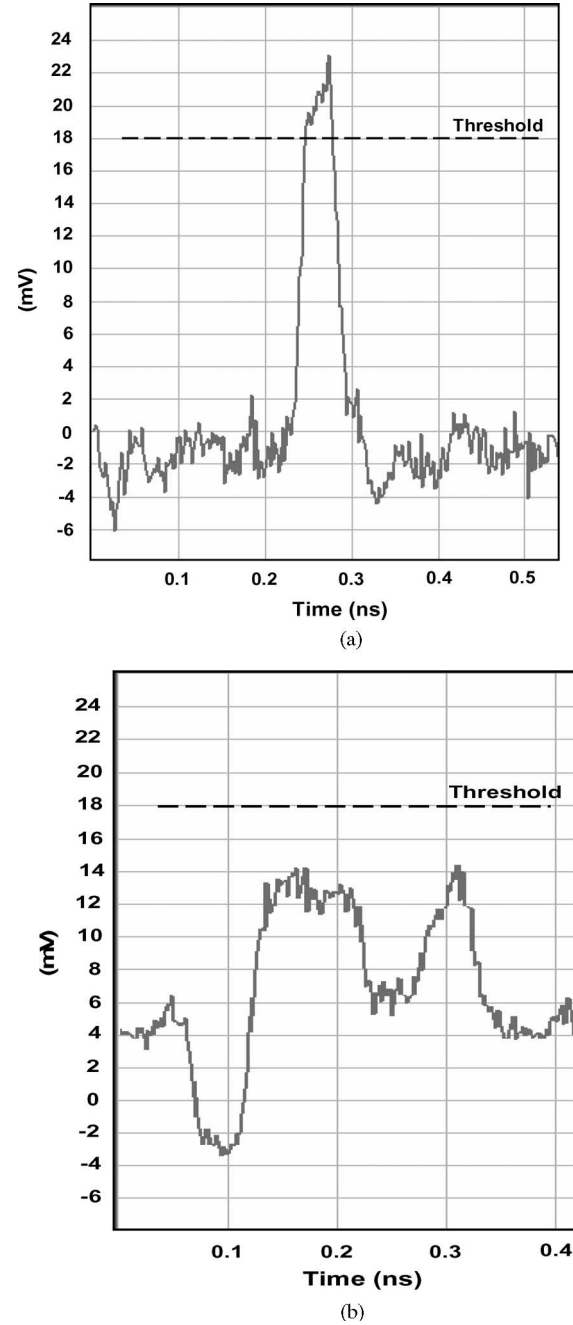


Fig. 5. Measured output waveform. (a) Autocorrelation when the wavelength profile matches the bit pattern 1011. (b) Crosscorrelation when the bit pattern does not match the wavelength profile.

increment of one bit-time (corresponding to the round-trip propagation between two Bragg gratings).

The delayed multiple wavelengths reflected off the Bragg gratings were routed through an optical circulator, and amplified using an erbium-doped fibre amplifier (EDFA). The wavelengths were then routed (by the second circulator) to a 1-mm diameter collimator, and the collimated beam was launched toward a blazed grating of 1200 lines/mm grating surface. The latter spread the wavelengths along different direction, and mapped them onto the active window of the Opto-VLSI, which was

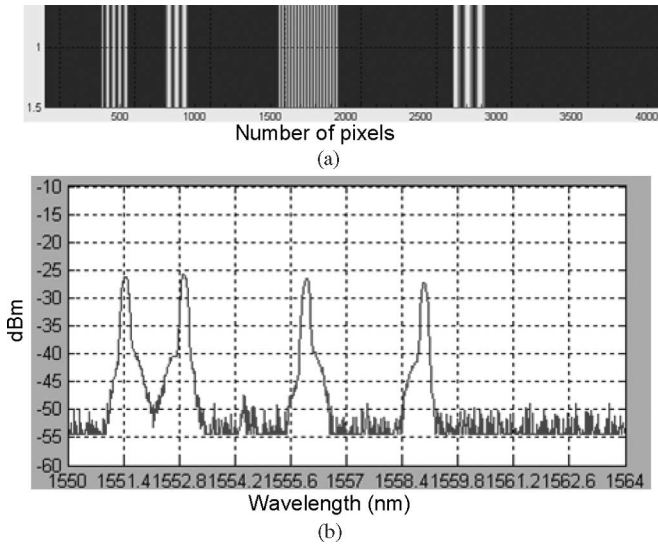


Fig. 6. (a) Opto-VLSI digital hologram of the pixel blocks to generate 110101 wavelength profile. (b) Wavelength profile that matches the optical bit pattern 110101.

logically partitioned into several pixel blocks that appropriately attenuate the different wavelength components to generate a wavelength profile that matches the bit pattern.

The Opto-VLSI processor used in the experiments had 1×4096 pixels. 256-level phase holograms were generated by applying appropriate voltage levels between 0 V and 2 V to the individual pixels. A program was written in MATLAB to generate, and send command voltages in the form of image to the Opto-VLSI processor to generate optimized steering holograms for the incident wavebands. The program allowed the user to steer many input channels, each independently controlled in terms of position, width, and phase profile. The initial phase hologram used for the real-time optimization procedure was a blazed grating. More information about the optimization algorithm for equalizing the wavelength power can be found in [19].

Each wavelength band was allocated a pixel block that was independently addressed to be either reflected back along its incident optical path, hence, coupled into the fibre collimator with minimum attenuation, or appropriately steered away so its power is not coupled back into the fibre collimator, leading to independently-controlled optical attenuation for each wavelength band. The coupled-back optical signal was detected by the high-speed photodetector, and the detected waveform was displayed on a high-speed oscilloscope.

A. Four-bit Pattern Recognition Demonstration

An Anritsu pattern generator was used to generate a 4-bit packet 1011 at 10 Gbit/s, and the Opto-VLSI processor was loaded with wavelength profile which matches the input bit-pattern as shown in Fig. 4. Fig. 4(a) shows the steering digital phase hologram, which coupled the wavelength components λ_1, λ_3 , and λ_4 , and steered away the other wavelength components, generating a wavelength profile 1011 as shown in Fig. 4(b). The coupled-back optical signal was detected by the high-speed photodetector. Fig. 5(a) shows the measured wave-

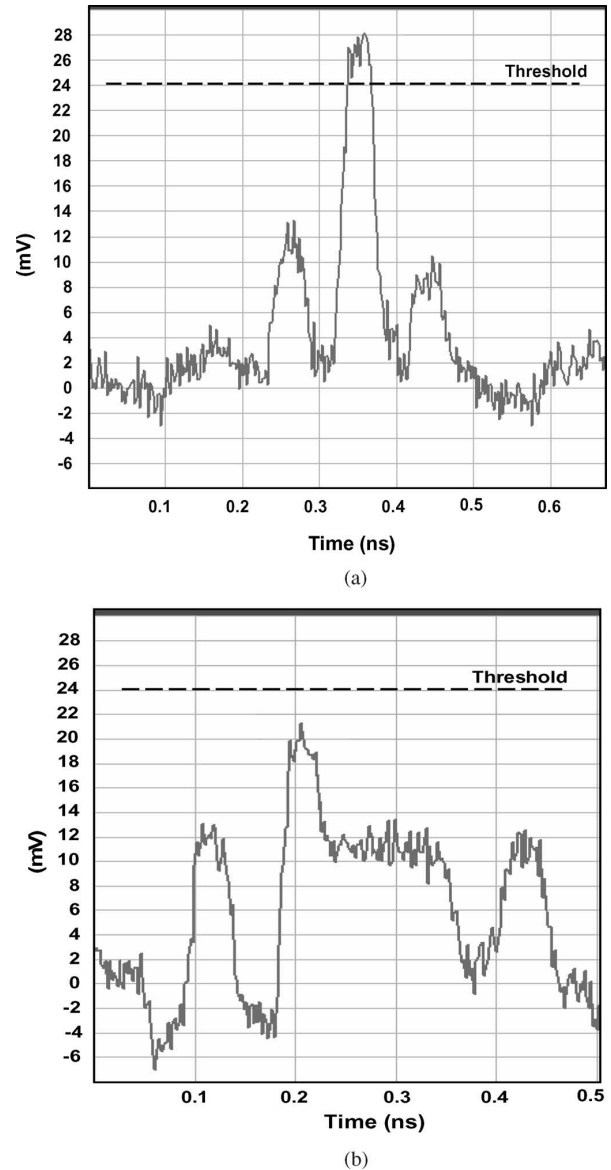


Fig. 7. Measured output waveform. (a) Autocorrelation when the wavelength profile matches the bit pattern 110101. (b) Crosscorrelation when the bit pattern does not match the wavelength profile.

form, which corresponds to an autocorrelation with a high-peak at the centre, which is due to matching between the wavelength profile and the bit pattern.

However, when the bit pattern mismatches the wavelength profile, a crosscorrelation was generated as shown in Fig. 5(b) where the input pattern was changed to 1101 and the wavelength profile was left without change.

B. Six-bit Recognition Demonstration

For this scenario, the 110101 bit pattern at 10 Gb/s was generated and the Opto-VLSI was loaded with the proper hologram to generate a matched wavelength profile. Fig. 6(a) shows the digital phase hologram and Fig. 6(b) shows the wavelength profile that matches the 110101 bit pattern. The coupled-back signal was detected using the photodetector, and an autocorrelation

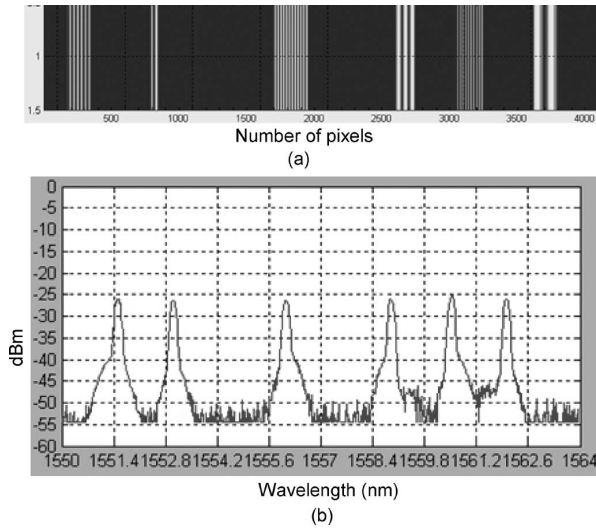


Fig. 8. (a) Opto-VLSI digital hologram of the pixel blocks to generate 11010111 wavelength profile. (b) Wavelength profile that matches the optical bit pattern 11010111.

function was generated as shown in Fig. 7(a). When the bit pattern changed to 101011, a crosscorrelation function was generated as displayed in Fig. 7(b).

C. Eight-bit Pattern Recognition Demonstration

The 8-bit pattern 11010111 was generated at 10 Gbit/s. To match this bit pattern, the Opto-VLSI was driven with the digital phase hologram shown in Fig. 8(a), which generated a wavelength profile that matches the bit pattern as shown in Fig. 8(b). As a result, an autocorrelation function was generated with a high-peak as shown in Fig. 9(a). Changing the input pattern to 10101011 resulted in the crosscorrelation waveform shown in Fig. 9(b).

VI. DISCUSSION

The results shown in Figs. 4–9 show the capability of the proposed multiwavelength header/label recognition structure to reconfigure its wavelength profile, enabling the recognition of arbitrary bit patterns. This is mainly due to the unique features of Opto-VLSI processors, which include wide wavelength range of operation, the ability to synthesise a lookup table of wavelength profiles that match arbitrary patterns, and transparency to data bit-rate. Unlike all other reported all-optical header/label recognition that are designed for fixed data bit-rates, the present structure is attractive for dynamic packet switched networks operating at different data bit-rates.

The lookup table of the proposed multiwavelength header recognition structure is constructed using an Opto-VLSI processor which generates multiwavelength profiles using digital phase holograms for recognizing different headers. Reported optical header recognition structures are bit-rate dependent because they require FBG elements spaced accurately for a specific data bit-rate, and hence, these structures must entirely be changed as the bit-rate and/or the number of header bits change. On the contrary, an Opto-VLSI processor can generate recon-

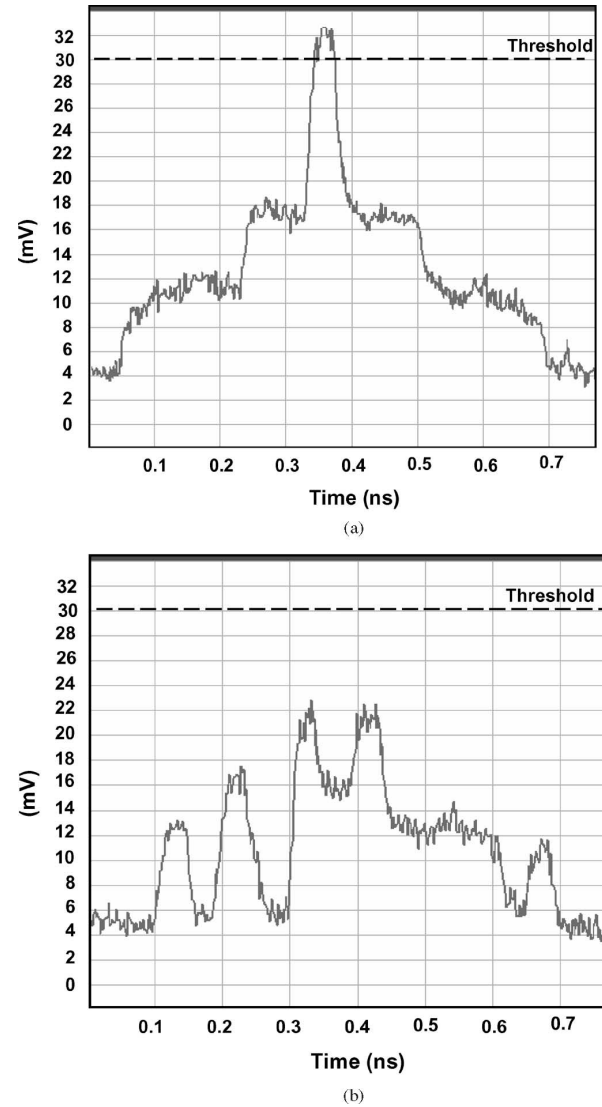


Fig. 9. Measured output waveform. (a) Autocorrelation when the wavelength profile matches the bit pattern 11010111. (b) Crosscorrelation when the bit pattern (10101011) does not match the wavelength profile (11010111).

figurable multiwavelength profiles of arbitrary bit lengths that are independent of the bit-rate. Thus, the same Opto-VLSI processor can be used as a lookup table for different bit-rates. Note that, when the data bit-rate is changed, only the ASE slicing FBG array needs to be changed to match the new bit-rate, whereas no change to the lookup table is needed.

To produce a good correlation waveform it is necessary to equalize the intensities of the output wavelength components. This can be realized through phase hologram optimization. As noted from the Sections IV-A–C, the phase holograms that control similar wavelengths are not the same for all the three scenarios. This is because of the above mentioned multiwavelength equalization.

In addition, it is important to note that if a no-match pattern generated a high crosscorrelation, an error-free header recognition can be accomplished by adding a second correlator, configured in complement to the first correlator, in conjunction with an

AND gate so that a ZERO is produced at the centre of the output when the pattern matches the gain profile and ONE otherwise, as reported by Hauer *et al.* [4].

Note that the use of an ASE source is more efficient and cost-effective in comparison to the use of several DFB laser sources. The only drawback of slicing an ASE source is the reduced power per waveband. However, this can be easily overcome using an EDFA that produces adequate power level per waveband.

The scalability of the proposed multiwavelength header/label recognition structure depends on the size of the active window and the bandwidth of the Opto-VLSI processor. The active window of the Opto-VLSI processor can practically be as large as 20 mm \times 20 mm. For a pixel size of 5 μ m \times 5 μ m, 4000 \times 4000 pixel Opto-VLSI processors can practically be fabricated. Using pixel blocks of 64 \times 64 pixels and a dead space of 64 pixels, headers of 32 bits can be realised. Moreover, Opto-VLSI processors have optical bandwidths exceeding 80 nm, thus, the proposed correlator architecture can be scaled 100 Gb/s and beyond.

The dispersion caused by the Opto-VLSI (being a diffractive element) was experimentally investigated to ensure that the optical header recognition is not degraded by the pulse broadening. The measured pulse broadening was less than 0.01 ns, hence, the measured dispersion caused by the Opto-VLSI processor was negligible.

VII. CONCLUSION

A reconfigurable 4-, 6-, and 8-bit pattern multiwavelength header/label recognition structure has been experimentally demonstrated at 10 Gb/s. The proposed structure employs a single Opto-VLSI processor and an array of FBG. Each bit pattern in the lookup table has been represented by a wavelength profile generated using digital phase holograms. An autocorrelation function of a high-peak has been generated whenever the bit pattern matched the wavelength profile. Measured autocorrelation and crosscorrelation waveforms of different bit pattern lengths have demonstrated the capability of the proposed correlator to recognize arbitrary bit patterns. The proposed structure can be scaled to more bit pattern by using an Opto-VLSI processor with a large active window.

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Kiegon Im, photograph and biography not available at the time of publication.

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